IN THE CLAIMS

1-18. (Canceled)

19. (Previously Presented) A method of using a floating gate transistor having a floating gate electrode and an adjacent amorphous silicon carbide (a-SiC) gate insulator between the floating gate electrode and a substrate, the method comprising:

storing data by changing a charge of the floating gate electrode;

reading data by detecting a current between a source and a drain in the substrate; and

refreshing data based on a data charge retention time for the floating gate transistor that depends upon a barrier energy at an interface between the floating gate electrode and the gate insulator.

20. (Previously Presented) The method of claim 19, wherein reading data further comprises detecting an amplified current signal between the source and the drain.

21. (Previously Presented) The method of claim 19, wherein the detected current is based on the charge of the floating gate electrode and a transconductance gain of the floating gate transistor.

22-27. (Canceled)

28. (Previously Presented) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV; and

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate.

29. (Previously Presented) The method of claim 28 wherein programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode.

30. (Previously Presented) The method of claim 28, further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

31. (Previously Presented) The method of claim 28, further comprising refreshing the charge placed on the floating gate electrode.

32. (Previously Presented) The method of claim 31, wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals of less than 40 seconds.

33. (Previously Presented) The method of claim 31, wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals.

34. (Previously Presented) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

storing data on a floating gate electrode in the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line such that charge is carried from a substrate to the floating gate electrode through a silicon carbide (SiC) gate insulator, wherein a barrier energy between the silicon carbide (SiC) gate insulator and the floating gate electrode is less than 3.3 eV;

reading the data stored on the floating gate electrode by placing a read voltage on the control line and detecting the current in the floating gate transistor at the data line; and

erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

35. (Previously Presented) The method of claim 34 wherein storing data further comprises causing the charge to be carried from the substrate to the floating gate electrode through an amorphous silicon carbide (a-SiC) gate insulator.

36. (Previously Presented) The method of claim 34, further comprising refreshing the charge placed on the floating gate electrode.

37. (Previously Presented) The method of claim 36 wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals of less than 40 seconds.

38. (Previously Presented) The method of claim 36 wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals.

39-42. (Canceled)

43. (Previously Presented) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

44. (Previously Presented) The method of claim 43 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

45. (Previously Presented) The method of claim 43, further comprising reading the floating gate transistor by detecting current in the floating gate transistor.

46. (Previously Presented) The method of claim 43, further comprising refreshing the floating gate transistor at regular time intervals.

47. (Previously Presented) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

48. (Previously Presented) The method of claim 47 wherein:

programming comprises programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor; and

erasing comprises applying an erase voltage of less than 12 Volts to the floating gate transistor to erase the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling.

49. (Previously Presented) The method of claim 47, further comprising reading the floating gate transistor by placing a read voltage on the control line and detecting current in the floating gate transistor.

50. (Previously Presented) The method of claim 47, further comprising refreshing the floating gate transistor at regular time intervals of less than 40 seconds.

51. (Previously Presented) The method of claim 19 wherein reading data comprises reading data by detecting a current between a source and a drain in a silicon substrate.

52. (Previously Presented) The method of claim 43 wherein programming comprises programming the floating gate transistor by inducing charge to migrate from a channel between a source and a drain in a silicon substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor.

53. (Previously Presented) The method of claim 47 wherein programming comprises programming the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line to induce charge to migrate from a channel between a source and a drain in a silicon substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor.

54. (Previously Presented) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and an amorphous silicon carbide (a-SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV; and

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate.

55. (Previously Presented) The method of claim 54, further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

56. (Previously Presented) The method of claim 54, further comprising refreshing the charge placed on the floating gate electrode.

57. (Previously Presented) The method of claim 56, wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals.

58. (Previously Presented) The method of claim 54 wherein programming further comprises programming the floating gate electrode by inducing charge to migrate from a channel between a source region and a drain region in a silicon substrate through the amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode.

59. (Previously Presented) A method for operating a floating gate transistor connected to a control line and a data line, the method comprising:

storing data on a floating gate electrode in the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line such that charge is carried from a substrate to the floating gate electrode through an amorphous silicon carbide (a-SiC) gate insulator, wherein a barrier energy between the amorphous silicon carbide (a-SiC) gate insulator and the floating gate electrode is less than 3.3 eV;

reading the data stored on the floating gate electrode by placing a read voltage on the control line and detecting the current in the floating gate transistor at the data line; and

erasing the floating gate transistor by applying an erase voltage to the floating gate transistor.

60. (Previously Presented) The method of claim 59, further comprising refreshing the charge placed on the floating gate electrode.

61. (Previously Presented) The method of claim 60 wherein refreshing the charge placed on the floating gate electrode further comprises refreshing the charge at regular time intervals.

62. (Previously Presented) The method of claim 59 wherein erasing comprises erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

63. (Previously Presented) The method of claim 59 wherein storing data further comprises storing data on the floating gate electrode in the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line such that charge is carried from a channel between a source region and a drain region in a silicon substrate to the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator.

64. (Previously Presented) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV;

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate; and

erasing the floating gate transistor.

65. (Previously Presented) The method of claim 64 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

erasing the floating gate transistor comprises erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts; and

further comprising refreshing the charge placed on the floating gate electrode at regular time intervals.

66. (Previously Presented) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV;

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate; and

refreshing the charge placed on the floating gate electrode.

67. (Previously Presented) The method of claim 66 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

refreshing the charge comprises refreshing the charge placed on the floating gate electrode at regular time intervals; and

further comprising erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

68. (Previously Presented) A method of using a floating gate transistor, comprising:

programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate, the barrier energy being less than approximately 3.3 eV;

reading the floating gate transistor by placing a read voltage on a control gate and detecting current in a channel between a source region and a drain region in the substrate;

refreshing the charge placed on the floating gate electrode; and

erasing the floating gate transistor.

69. (Previously Presented) The method of claim 68 wherein:

programming a floating gate electrode further comprises causing hot electron injection from the channel through an amorphous silicon carbide (a-SiC) gate insulator to the floating gate electrode;

refreshing the charge comprises refreshing the charge placed on the floating gate electrode at regular time intervals; and

erasing the floating gate transistor comprises erasing the floating gate transistor by applying an erase voltage to the floating gate transistor which is less than 12 Volts.

70. (Previously Presented) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

reading the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

71. (Previously Presented) The method of claim 70 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

reading the floating gate transistor comprises reading the floating gate transistor by detecting current in the floating gate transistor;

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling; and

further comprising refreshing the floating gate transistor at regular time intervals.

72. (Previously Presented) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

refreshing the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

73. (Previously Presented) The method of claim 72 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling;

refreshing the floating gate transistor comprises refreshing the floating gate transistor at regular time intervals; and

further comprising reading the floating gate transistor by detecting current in the floating gate transistor.

74. (Previously Presented) A method for operating a floating gate transistor comprising:

programming the floating gate transistor by inducing charge to migrate from a channel in a substrate through an amorphous silicon carbide (a-SiC) gate insulator to a floating gate electrode in the floating gate transistor;

refreshing the floating gate transistor;

reading the floating gate transistor; and

erasing the floating gate transistor by inducing charge to migrate from the floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel.

75. (Previously Presented) The method of claim 74 wherein:

programming comprises programming the floating gate transistor by inducing hot electron injection from a channel in a substrate through the amorphous silicon carbide (a-SiC) gate insulator to a polysilicon floating gate electrode in the floating gate transistor;

erasing comprises erasing the floating gate transistor by inducing charge to migrate from the polysilicon floating gate electrode through the amorphous silicon carbide (a-SiC) gate insulator to the channel through Fowler-Nordheim tunneling; and

refreshing the floating gate transistor comprises refreshing the floating gate transistor at regular time intervals; and

reading the floating gate transistor comprises reading the floating gate transistor by detecting current in the floating gate transistor.